Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

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**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: G = .035” X .044”**

**Backside Potential: DRAIN**

**Mask Ref: IX7N**

**APPROVED BY: DK DIE SIZE .288” X .303” DATE: 6/1/22**

**MFG: IXYS THICKNESS .012” P/N: IXTD20N50D**

**DG 10.1.2**

#### Rev B, 7/1